Information Disclosure Statements

The applicant submitted an Information Disclosure Statement on August 14, 1998. Supplemental Information Disclosure Statements were filed on October 28, 1998 and June 25, 1999. The applicant respectfully requests that these Information Disclosure Statements be entered and the documents listed on the attached Forms 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of each of the forms 1449, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Rejections under 35 USC §103

Ukai et al.

Claims 43-45, 47, and 49 were rejected under 35 USC § 103(a) as being unpatentable over Ukai et al. (U.S. Patent No. 4,849,797, Ukai). The applicant respectfully traverses.

Claim 43 recites a method for operating a floating gate transistor including, among other elements, programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through a gate insulator to a floating gate electrode.

Ukai is deficient in the following respects. Ukai discloses a thin film transistor in Figure 6 sitting on top of a substrate 11. Charge transfer takes place across an active layer 19 between a source 14 and a drain 15. A gate electrode 18 is separated from the active layer 19 by a gate insulating film 23 to control the charge transfer in the active layer 19. However, Ukai does not disclose a floating gate transistor, or a method including inducing charge to migrate from a channel in a substrate through a gate insulator to a floating gate electrode. The gate electrode 18 is a control gate, not a floating gate.

Furthermore, in the transistor of Ukai no channel is formed in the substrate 11. In the Figures of Ukai six semiconductor structures are shown, each with a substrate 11. The substrate 11 is described in column 1, lines 18-20, as an "insulating substrate 11 of glass or similar material." No channel may be formed in a substrate that is an insulator.

The suggestions of the Examiner do not supply the elements missing in Ukai. Therefore, the applicant respectfully submits that claim 43 is not disclosed or suggested by Ukai. For the

reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 44 and 45, which are dependent on claim 43, are also not disclosed or suggested by Ukai.

Claims 47 and 49 recite elements similar to those recited in claims 43 and 45. For reasons analogous to those state above, and the limitations in the claims, the applicant respectfully submits that claims 47 and 49 are also not disclosed or suggested by Ukai.

Sugita et al.

Claims 19-21, 43-47, and 49 were rejected under 35 USC § 103(a) as being unpatentable over Sugita et al. (JP Patent No. 08-255878, Sugita). The applicant has submitted an English translation of Sugita in the information disclosure statement filed on June 25, 1999. The applicant respectfully traverses.

Claim 19 recites a method of using a floating gate transistor having a floating gate electrode and an adjacent amorphous silicon carbide (a-SiC) gate insulator between the floating gate electrode and a substrate.

Sugita is deficient in the following respects. Sugita discloses in Figure 1 a floating gate transistor with a Beta-Silicon Carbide film 5 between a substrate 1 and a floating gate 6. However, Sugita does not disclose an amorphous silicon carbide (a-SiC) gate insulator. The suggestions of the Examiner do not supply the elements missing in Sugita. Therefore, the applicant respectfully submits that claim 19 is not disclosed or suggested by Sugita. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 20 and 21, which are dependent on claim 19, are also not disclosed or suggested by Sugita.

Claims 43-47 and 49 recite elements similar to those recited in claims 19-21. For reasons analogous to those state above, and the limitations in the claims, the applicant respectfully submits that claims 43-47 and 49 are also not disclosed or suggested by Sugita.

New Claims

The applicant has added new claims 43-50, and respectfully submits that all of the new claims 43-50 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 10/12/99 By _____
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **October 12, 1999**.

Tina Pugh
Name

Tina Pugh
Signature